

The Open Systems Digital Technology Laboratory is a research and development laboratory to develop COTS based System Integration Technologies and apply these technologies to Mission and Vehicle Avionics. The facility contains various COTS technologies used to demonstrate system integration solutions and the demonstrations are then linked to ACETEF for avionic platform demonstrations.

Open Systems Digital Technology Laboratory

The Open Systems Digital Technology Lab demonstrates the feasibility of the extensive use of commercial opens system standards such as Fibre Channel, Futurebus+ and POSIX and COTS parts such as the PowerPC. These open system interfaces and commercial processors and parts will be inserted into existing avionics such as the AYK-14 architecture to demonstrate the dramatic increase in processing and I/O possible with these COTS parts.

The processing and I/O performance of existing aircraft, the F/A-18 and other advanced aircraft. must increase to meet the expanding mission roles of future combat scenarios. The present processing suite of existing aircrafts is inadequate to provide the required processing requirements of in-flight mission replanning, retargeting, automated mission management and common tactical picture-situation awareness (SA) displays. One of the key objectives of the Open Systems Digital Technology Lab is to increase the processing and I/O of the existing architecture by an order of magnitude.





(From the 2-4 MIPS range to the 100+ MIPS range and I/O rates from the 5 Mbit/s to the 250+ Mbit/s range.) The objective of the Open Systems Digital Technology Lab is to develop low-risk approaches to enhance existing avionics processing and I/O throughout for potential upgrades to the F/A-18 and other advanced aircraft. For instance, the Maritime Avionics Subsystems and Technology (MAST) Program, utilizing the resources of the Open Systems Digital Technology Lab, will demonstrate the insertion of high payoff avionics functionality into the F/A-18's existing wiring and architecture. This program will use the existing MIL-STD-1553 data bus architecture because of the prohibitive costs of a complete aircraft rewiring. The goal of MAST is to demonstrate the feasibility and

payoff of incrementally inserting new avionics functionality into the existing AYK-14 and the AAYK-14 architectures and the benefits of incrementally evolving these architectures from a closed federated architecture to a high performance, open system and networked based architecture.

Software integration components and techniques developed in the lab will provide a real-time, distributed operating system which uses defined interfaces between major layers and will be based on commercial interface standards such as POSIX. The operating system and distributed communication mechanisms will include support for a secure software system and enhanced system-level fault tolerance features.

For more information contact the Open Systems Digital Technology Laboratory at the Naval Air Warfare Center Aircraft Division, Patuxent River, MD at 301-342-2043.